REMARKS

Claims 1-7, 10-20 and 24-34 are pending in this application. Claims 8, 9 and 21-23 are canceled. Claims 24-34 are new. No new matter has been introduced.

The Examiner rejected claims 21-23 under 35 U.S.C. Section 112, first paragraph, as failing to comply with the enablement requirement. While Applicants respectfully disagree, Applicants have canceled claims 21-23 rendering the rejection moot.

THE CLAIMS ARE DIRECTED TO STATUTORY SUBJECT MATTER

The Examiner rejected claims 1-7 and 10-20 under 35 U.S.C. Section 101 as directed to non-statutory subject matter. Applicants respectfully traverse the Examiner's rejections. Applicants will address each of the independent claims in turn. The dependent claims are directed to statutory subject matter at least by virtue of their dependencies.

Independent claim 1, as amended, recites, "A linear scalable method of processing a digital signal under control of instructions executing on a multiprocessor computing system by computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) of the digital signal using a decimation in time approach, comprising the steps of: … storing the transformed signal in a memory." The Examiner contends that performing an FFT/IFFT is not a practical application. The claims, however, recite processing a digital signal by performing an FFT/IFFT. They do not recite performing an FFT/IFFT in a vacuum. Processing a digital signal is a practical application. Claim 1, as amended, recites a method for processing a digital signal that is performed using a multiprocessor system, and which includes storing of the results of the process in a memory. To the extent the Examiner contends processing digital signals is not useful unless a particular application for the digital signal is recited, Applicants respectfully submit that digital signal processing is itself a commercially useful application, and when coupled with the use of a machine to perform the recited method of digital signal processing, and further with storage of the processed signal in a memory, is a tangible application. The Examiner's position that digital signal processing on a multiprocessor system is not a useful, tangible application is inconsistent with the reality of the marketplace, where tangible digital signal processing systems are regularly bought and sold and are highly tangible and useful. Further, claim 1 does not preempt every application of the ideas because it is tied to use on a

particular system, a multiprocessing system. Nor is this a case where Applicants have failed to recite a specific process for performing the recited method using the multiprocessor system. Accordingly, claim 1 and the claims that depend therefrom are directed to statutory subject matter. With regard to new dependent claims 24-26, filtering, spectral analysis and polyphase transforming further limit the recited practical, tangible application of digital signal processing.

Independent claim 3, as amended, recites, "A linear scalable system to process a digital signal by computing a Fast Fourier Transform (FFT) or Inverse Fast Fourier transform (IFFT) of the signal in a multiprocessing system using a decimation in time approach, comprising: … means for distributing the butterfly operations … such that each processor computes… and a memory for storing inputs and output of the means for computing." As noted above, claim 3 recites computing an FFT or an IFFT of the digital signal, and transforming digital signals is a useful, tangible result. The Examiner also contends that claim 3 is a "software module." The Examiner's reasoning that means-plus-function language that could be performed by a software module is not patentable is inconsistent with claim 3, which recites "each processor computes …" and "a memory." Processors and memory are certainly hardware. Accordingly, claim 3 and the claims that depend therefrom are directed to statutory subject matter. Further, dependent claims 4 and 15 recite memory locations in the means for storing inputs and outputs, and thus are directed to statutory subject matter for this additional reason.

Independent claim 5, as amended, recites, "A computer-readable memory medium whose contents cause a system having a plurality of processors to perform a linear scalable method of transforming a signal by computing with the plurality of processors a Fast Fourier Transform (FFT) or an Inverse Fast Fourier Transform (IFFT) of the signal using a decimation in time approach, the method comprising …." The Examiner contends that claim 5 is software per se and there is no specific structure for carrying it out. A claim which involves a mental process and one of the other categories of statutory subject matter may be directed to statutory subject matter. Applicants have amended claim 5 to restate it in a computer readable memory medium format which Applicants believe may address some of the Examiner's concerns. To the extent the Examiner contends transforming a signal by computing an FFT/IFFT of the signal is not a

useful, tangible result, Applicants respectfully disagree for the reasons set forth above with respect to independent claim 1.

Independent claim 16, as amended, recites, "[a] computer-readable memory medium whose contents cause a system having a plurality of processors to perform a linear scalable method of transforming a signal, the method comprising …." Thus, claims 5 and 16 are directed to a useful application (signal processing) tied to another category of statutory subject matter (a composition, namely a computer-readable memory medium). Both claims further indicate that the transformed signal is stored. Further, the claims indicate the computer-readable medium is intended for use in a processing system. Accordingly, claims 5 and 16 and the claims that depend respectively therefrom are directed to statutory subject matter.

New independent claim 27 recites, "A method of transforming a digital signal … comprising: computing, with a multiprocessor system having a plurality of processors P … and storing the transformed signal in a memory medium." As discussed above, transforming a digital signal is a useful tangible result and the method is tied to a plurality of processors and a memory, which are hardware. Thus, new claim 27, as well as dependent claims 28-30, are directed to statutory subject matter.

New independent claim 31 recites, "A system, comprising: an instruction fetch cache; and a plurality P processors coupled to the instruction fetch catch configured to: compute a first number of butterfly stages of an N-point Fast Fourier Transform (FFT) or Inverse Fast Fourier Transform (IFFT) of a digital signal." A system comprising an instruction fetch cache and a plurality of processors is hardware, and computing an FFT/IFFT of a digital signal is useful. Thus claim 31, as well as claims 32-34 that depend from claim 31, are directed to statutory subject matter.

THE CLAIMS ARE NOT RENDERED OBVIOUS BY ABEL AND JABER

The Examiner rejected claims 1-7 and 10-20 under 35 U.S.C. Section 103(a) as rendered obvious over U.S. Patent No. 5,991,787 issued to Abel, et al., in view of U.S. Patent No. 6,792,441 issued to Jaber. Applicants respectfully traverse the Examiner's rejections.

Applicants previously argued that Abel was not an appropriate primary reference because the claims in the present application are directed to linearly scalable methods, systems

and products for computing FFTs or inverse FFTs on multiprocessor systems, while Abel is directed to reducing peak spectral error for a specific processor, namely an MMX™ processor, using a specific instruction set and configuration. Abel reduces peak spectral error using rounding. Abel is not directed to linear scalability. Thus, the Examiner's assertion that Abel discloses "a linear scalable method" is incorrect.

The Examiner contends that the definition of linear scalability in the specification does not appear in the claims. The Federal Circuit has made it clear that a patentee may serve as its own lexicographer, and thus may define in the specification terms as used in the claims. *Sinorgchem Co. Shandong v. Int'l Trade Comm.*, 511 F.3d 1132, 1136 (Fed. Cir. 2007) ("Our opinions have repeatedly encouraged claim drafters who choose to act as their own lexicographers to clearly define claim terms used in the claims in the specification) (holding International Trade Commission erred in ignoring portions of the definition of a claim term contained in the specification). Thus, the Examiner's position that "linear scalable" will be giving no weight in the claims because the claims do not contain the definition set forth in the specification is an unreasonable interpretation of the claim language.

The Examiner points to Figure 7 of Abel as disclosing linear scalability. Specifically, the Examiner contends Figure 7 shows "input coefficients can be any size." The specification of the present application defines linear scalability as "the computation time reducing in inverse proportion to the number of processors in the multiprocessor solution." Specification at page 3, lines 11-14. Even assuming Figure 7 somehow shows that input coefficients can be any size (it does not, and the Examiner has failed to provide support for any argument that "input coefficients can be any size" is inherent in Figure 7), Figure 7 of Abel and the description thereof do not address linear scalability of a multi-processor system. Thus, Applicants continue to contend that Abel is not an appropriate primary reference because it does not address linear scalability. Further, Jaber is directed to specific hardware architectures, and is not directed to achieving linear scalability. Thus one would not be motivated to combine Abel and Jaber to obtain linear scalability in a multiprocessor system.

Further, the claimed invention uses a plurality of processors to perform a plurality of butterfly computations similar to the architecture claimed by Jaber. However, the present

method does not necessitate the use of a "combination phase" used by Jaber, as shown in Fig 8 (component 817), Fig 9 (components 907, 909, 913A, 916 etc), Fig 10 right side, Fig 11 right side and Column 3 last paragraph. It is not obvious how the method outlined in the claims could be derived from Jaber's teachings without use of the said combination phase.

Turning to the language of the claims, claim 1 as amended recites, "A linear scalable method … comprising … computing an N-point FFT/IFFT of the signal using a first plurality of butterfly computational stages, each stage in the first plurality of stages employing a plurality of butterfly operations having a first radix, wherein each of the butterfly operations in each stage in the first plurality of stages has a single, un-nested computation loop of the first radix; distributing the plurality of butterfly operations in each stage of the first plurality of stages such that each processor computes an equal number of complete butterfly operations thereby eliminating data interdependency in the stage." Claim 16 recites similar language. Neither Abel nor Jaber teach, suggest or motivate a linear scalable method comprising a first plurality of stages employing a plurality of butterfly operations having a first radix, wherein each of the butterfly operations in each stage in the first plurality of stages has a single, un-nested computation loop of the first radix, as recited. Accordingly, claims 1 and 16 are not rendered obvious by Abel, alone or in combination with Jaber. Claims 2, 7, 10, 11 and 24-26 depend from claim 1 and claims 17-20 depend from claim 16, and are allowable at least by virtue of their dependencies.

Claim 3, as amended, recites, "[a] linear scalable system … comprising: means for computing a plurality of stages of an N-point FFT/IFFT using in each stage of the plurality of stages a plurality of butterfly operations, wherein each butterfly operation employs a single butterfly computation loop of a first radix and without employing nested loops." Neither Abel nor Jaber teach, suggest or motivate a linear scalable system comprising: means for computing a plurality of stages of an N-point FFT/IFFT using in each stage of the plurality of stages a plurality of butterfly operations, wherein each butterfly operation employs a single butterfly computation loop of a first radix and without employing nested loops, as recited. Accordingly, claim 3 is not rendered obvious by Abel, alone or in combination with Jabar. Claims 4 and 12-15 depend from claim 3, and are allowable at least by virtue of their dependencies.

Claim 5, as amended, recites, "A computer-readable memory medium whose contents cause a system having a plurality of processors to perform a linear scalable method of transforming a signal by computing with the plurality of processors a Fast Fourier Transform (FFT) or an Inverse Fast Fourier Transform (IFFT) of the signal using a decimation in time approach, the method comprising: computing first and second stages of $\log_2 N$ stages of an N-point FFT/IFFT as a single radix-4 butterfly operation while implementing the remaining ($\log_2 N$-2) stages using radix-2 butterfly operations, wherein each radix-2 butterfly operation employs a single radix-2 butterfly computation loop without employing nested loops." As mentioned above, neither Abel nor Jaber teach, suggest or motivate a linear scalable method. Thus, claim 5 is not rendered obvious by Abel, alone or in combination with Jaber. Claim 6 depends from claim 5 and is allowable at least by virtue of its dependency. Accordingly, claims 1-20 are not rendered obvious by Abel, alone or in combination with Jaber.

New claim 27 recites, "A method of transforming a digital signal, the method comprising … computing remaining butterfly stages of the N-point FFT/IFFT with a single iterative loop wherein each butterfly operation in each stage of a loop iteration is computed on a single respective processor in the plurality of processors and there is no data dependency between butterflies in a stage of an iteration of the loop." Abel, alone or in combination with Jaber, does not teach, suggest or motivate computing remaining butterfly stages of an N-point FFT/IFFT with a single iterative loop wherein each butterfly operation in each stage of a loop iteration is computed on a single respective processor in a plurality of processors and there is no data dependency between butterflies in a stage of an iteration of the loop. Acccordingly, claim 27, as well as claims 28-30 that depend from claim 27, are not rendered obvious by Abel in view of Jaber.

New claim 31 recites, "A system, comprising … a plurality P processors coupled to the instruction fetch catch and configured to … compute remaining butterfly stages of the N-point FFT/IFFT with a single iterative loop wherein each butterfly operation in each stage of a loop iteration is computed on a single respective processor in the plurality of processors and there is no data dependency between butterflies in a stage of an iteration of the loop." Abel, alone or in combination with Jaber, does not teach suggest or motivate a plurality P processors

configured to compute remaining butterfly stages of an N-point FFT/IFFT with a single iterative loop wherein each butterfly operation in each stage of a loop iteration is computed on a single respective processor in the plurality of processors and there is no data dependency between butterflies in a stage of an iteration of the loop. Accordingly, claim 31, as well as claims 32-34 that depend from claim 31, are not rendered obvious by Abel in view of Jaber.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC

/Timothy L. Boller/
Timothy L. Boller
Registration No. 47,435

TLB:lh

701 Fifth Avenue, Suite 5400
Seattle, Washington 98104
Phone: (206) 622-4900
Fax: (206) 682-6031

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